REMARKS

Claims 1-26 remain pending in the application. Claims 1, 13, 14, and 15 have been amended.

35 U.S.C. § 102 and § 103 Rejections:

Claims 1-5, 9, 12 15-21, 23, and 26 were rejected under 35 U.S.C. § 102(e) as being anticipated by Olgaard, U.S. Patent 6,236,278. Claim 6 was rejected under 35 U.S.C. § 103(a) as being unpatentable over Olgaard in view of Han, U.S. Patent Application Publication 2003/0108143. Claims 7-8 were rejected under 35 U.S.C. § 103(a) as being unpatentable over Olgaard in view of Humphreys, U.S. Patent Application Publication 2002/0198912. Claims 11, 14, and 25 were rejected under 35 U.S.C. § 103(a) as being unpatentable over Olgaard in view of Lee, U.S. Patent Application Publication 2002/0025778. Claim 13 was rejected under 35 U.S.C. 103(a) Olgaard in view of Harpham, U.S. Patent Application Publication 2001/0017572. Claims 10 and 24 were rejected under 35 U.S.C. § 103(a) as being unpatentable over Olgaard in view of Takeuchi, U.S. Patent 5,521,948. Claim 22 was rejected under 35 U.S.C. §103(a) as being unpatentable over Olgaard in view of Kasturia, U.S. Patent 5,572,168. Applicant respectfully traverses these rejections.

With regard to the § 102 rejection, **the cited reference does not teach or suggest all of the elements of the independent claims**. Olgaard teaches a control circuit for causing a phase lock loop (PLL) frequency synthesizer to achieve a fast phase lock time while also providing improved loop performance during normal phase locked operation. The phase locking time of the PLL is minimized by initially configuring the PLL to operate in a fractional mode with high frequency signals presented to the inputs of the loop phase detector, thereby producing a fast phase lock time. Once the PLL has achieved phase lock, its operation mode is transitioned to either an integer mode or an open loop mode without loss of phase lock, thus causing lower frequency signals or no signals, respectively, to be presented to the inputs of the loop phase detector.

Independent claim 1 recites, in pertinent part:

"A phase locked loop device comprising ... an accumulator connected to said prescaler configured to provide a mode switching signal to said prescaler to switch between said at least two modes having assigned different prescaler factors, said accumulator storing an accumulator value, wherein said accumulator is adapted to repetitively update said accumulator value using a modulus function, to generate said mode switching signal to switch between said at least two modes having assigned different prescaler factors." (Emphasis added).

Independent claims 13, 14, and 15 recite similar combinations of features.

Olgaard does not teach or suggest this combination of features. In the office action, the Examiner contends that Olgaard teaches (referring to Fig. 6A and citing col. 7, line 43 to col. 8, line 67) that accumulator 670 and MOD 671 provide mode switching signal 654 to prescaler 655. Applicant respectfully disagrees with the Examiner's characterization of Olgaard's signal 654 and submits that this signal is not a mode switching signal as recited in the independent claims. In col. 8, lines 33-39, Olgaard states:

"If the modulus operation carried out during the given reference cycle results in an overflow ("OVF"), the OVF line 672 signals the cycle slip controller 652 to **add an extra N+1 divide** during the current reference cycle. This extra N+1 divide will occur after the auxiliary divider 651 has finished dividing by N+1 and has signaled the prescaler 665 to begin dividing by N." (Emphasis added).

In light of the above citation, Applicant submits that signal 654 (responsive to the OVF signal received by cycle slip controller 652) is used for adding an extra N+1 divide during the current reference cycle, which would thereby actually prolong the cycle by **preventing** the prescaler factor **from changing** to another prescaler factor. Accordingly, Applicant submits that signal 654 of Olgaard is the opposite of the mode switching signal recited in the independent claims, which causes a prescaler to switch between said at least

two modes having assigned **different** prescaler factors, as recited in the independent claims. Furthermore, Applicant can find no teaching or suggestion of an accumulator adapted to repetitively update the accumulator value using a modulus function to generate said mode switching signal, as recited in the independent claims. Accordingly, Applicant submits that Olgaard does not teach or suggest all of the elements of the independent claims and therefore respectfully requests removal of the 35 U.S.C. § 102(e) rejection.

With regard to the various § 103(a) rejections, Applicant submits that, for at least the reasons stated above with regard to the § 102(e) rejection, the cited references, taken singly or in combination, do not teach or suggest all of the elements of the independent claims. Accordingly, removal of the 35 U.S.C. §103(a) rejections is respectfully requested.

CONCLUSION

Applicant submits the application is in condition for allowance, and an early notice to that effect is requested.

If any fees are due, the Commissioner is authorized to charge said fees to Meyertons, Hood, Kivlin, Kowert, & Goetzel, P.C. Deposit Account No. 501505/5500-86101/EAH.

Respectfully submitted,

Erik A. Heter
Reg. No. 50,652
AGENT FOR APPLICANT(S)

Meyertons, Hood, Kivlin, Kowert, & Goetzel, P.C.
P.O. Box 398
Austin, TX 78767-0398
Phone: (512) 853-8800

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